I claim:

1. A method of mass-producing a solid state device comprising:

supplying a solid state material substrate having a top surface; and

providing a solid state material layer no more than 40 Angstroms thick having at least one atomically smooth major surface, and positioned on the top surface of the substrate;

at least a lower surface of the solid state material layer being metallurgically bonded onto a selected portion of the top surface of the solid state material substrate, sufficiently uniformly and defect-freely to provide an acceptable device yield.

2. The method as in claim 1 wherein the solid state material layer has at least two of the following features: a) having an atomically smoothed bottom surface; b) having a curved top surface; c) having an atomically smooth gate bottom surface; d) made of a solid state material purified during device processing; e) made of a single strengthened material; f) has uniformly oriented elongated and narrow grains; g) is stronger than unbonded device material; and h) less than two atomic layers thick.

3. The method as in claim 1 wherein the solid state material layer has a central bottom portion of zero width.

4. The method as in claim 1 wherein the solid state material layer has an accuracy of better than a single atom on a layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical

composition profiling, and lateral location.

5 The method as in claim 1 where at least a portion of the solid state material layer is surfaced strengthened, whereby this surface-strengthened portion is stronger than the unbonded solid state material layer itself.

6. The method as in claim 1 where the solid state material layer is sufficiently thin and flexible to yield under stress preventing device failure.

7. The method as in claim 1 wherein the solid state material layer is a liquid-diffusion aged or burned-in solid state material.

8. The method as in claim 1 wherein the device has a thickness of substantially less than a micron forming a flexible thin-film integrated circuit device.

9. The method as in claim 1 wherein the solid state material layer has a curved major surface with a radius of curvature of less than 1 micron.

10. The method as in claim 1 wherein material of the solid state material layer is at least one order of magnitude purer than the solid state material prior to the uniform metallurgical bonding.

11. The method as in claim 1 wherein the solid state material layer has an accuracy in thickness of two atomic or molecular layers.

12. The method as in claim 1 wherein the solid state material layer comprises an ion implanted region containing a material selected from the group consisting of oxygen and nitrogen.

13. The method as in claim 1 including:

providing a solid state material substrate having a common top surface;

supplying a first and a second solid state material pockets; and

positioning a first and a second solid state material pockets adjacent to each other, but laterally separated by a gap, on the common top surface of the substrate;

the solid state material layer filling and bridging the gap between the two adjacent solid state material pockets;

14. The method as in claim 13 wherein:

at least a part of the substrate is a semiconductor of a first conductivity type; and

at least one of the semiconductor material pockets is of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at least one semiconductor material pocket.

15. The method as in claim 1 wherein the solid state material layer is selected from the group consisting of a single-material gate layer and a single-material field layer.

16. The method as in claim 1 wherein the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

17. The method as in claim 1 wherein the device is selected from the group consisting of metal-oxide-semiconductor (MOS) device, conductor-insulator-semiconductor

(CIS) device, thin-film integrated circuit, flexible integrated circuit, electro optical device, single-electron device, single-hole device, single-carrier device, single-photon device, electrooptomagnetic devices and mixtures thereof.

18. The method as in claim 14 wherein:

the first and second semiconductor material pockets are respectively source and drain semiconductor pockets in a solid state device, and are separated by a gap from each other;

the solid state material layer is an electrically insulating gate layer filling and bridging the gap between the two pockets; and

the gate layer material has an atomically smooth surface on at least one of the top and major bottom surfaces thereof.

19. The method as in claim 13 wherein a major portion of each of the substrate, solid state material pockets, and solid state material layer consists essentially of a single semiconductor material doped to no more than 10 ppm of impurities thereby forming essentially a single-material device for resisting dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations.

20. The method as in claim 1 including forming a PN junction region having a curved adjoining surface uniformly and defect-freely bonded onto the substrate to thereby reduce but not eliminate at least one of thermal mismatch strain and volume change strain~~,~~

the remaining residual strain on the curved adjoining surface of the PN junction region improving a selected device

performance.

21. The method as in claim 14 wherein the at least one PN junction region has a bottom of zero width.

22. The method as in claim 1 wherein the solid state material layer is an electrically insulating, wavy and curved field layer containing a substance selected from the group consisting of oxygen and nitrogen.

23. The method as in claim 13 wherein:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a solid state device;

the solid state material layer is a single-material gate layer; and

including a conductive gate electrode of an electrically conducting material to control flow of electronic carriers from the source to the drain.

24. The method as in claim 23 wherein:

the solid state material layer is a gate layer which is atomically smooth and defect-free on at least the bottom major surface thereof;

material of the gate layer being purest at the bottom major surface facing the substrate.

25. The method as in claim 1 wherein the solid state material layer has a shallow, highly activated doped region having a significantly greater dopant concentration than the thermal equilibrium phase-diagram value.

26. The method as in claim 1 wherein the solid state material layer is a field layer separating and electrically isolating device components from each other;

the field layer on a horizontal cross-section thereof has a plurality of curved arc sections capable of changing arc lengths thereof to relieve thermal mismatch strains on the device.

27. A method for mass-producing a solid state device comprising:

supplying a solid state material substrate;

providing a solid state material pocket positioned on a selected surface of the substrate; and

forming a solid state material layer less than 40 angstroms thick and metallurgically bonded onto a selected surface of the substrate;

said metallurgical bonding being so sufficiently uniform and defect-free as to provide a thermochemically stable bonding interface and to give a manageable device yield.

28. The method as in claim 27 wherein the solid state material layer is selected from the group consisting of a gate layer and a field layer.

29. The method as in claim 27 wherein the solid state device is selected from the group consisting of atomic IC device, molecular IC device, single-electron device, single-hole device, single-carrier device, and single-photon device.

30. The method as in claim 27 wherein the solid state material layer has at least one of the following features: a) has a rounded bottom with zero width; b) has at least one atomically smooth major surface; c) bonded, atom to atom, onto the substrate; d) is purified by over one order of magnitude

during at least a device processing step; e) is surface strengthened; f) is liquid-diffusion formed; g) is formed using ion-implantation; h) is of an electrical insulating material; i) is free of voids and microcracks visible at 1,000 times magnification.

31. The method as in claim 27 including employing a real-time self-optimizing method to control, to an accuracy of 20 angstroms, a selected dimension of said solid state material layer;

said selected dimension being selected from the group consisting of length, width, thickness, location, shape, radius of curvature, and chemical composition profiling.

32. The method as in claim 31 including real-time sensing an optoelectcial signal from the solid state material layer.

33. A method for mass-producing a solid state device comprising:

supplying a solid state material substrate having a first conductivity type;

providing a solid state material pocket of a second conductivity type and positioned on a top surface of the substrate;

forming an interfacial rectifying barrier region where the solid state material pocket contacts the solid substrate; and

forming an electrically insulating solid state material layer no more than 40 angstroms wide and positioned on the substrate;

metallurgically bonding the solid state material layer onto both the pocket and the substrate; and

metallurgically bonding the solid state material layer onto selected portions of both the substrate and the pocket, sufficiently uniformly and defect-freely to achieve a manageable device yield; and

employing a real-time computerized automation method to optimize the metallurgical bonding  and to control dimensions of the solid state material pocket and layer both to an accuracy of better 20 angstroms.

34. The method as in claim 33 including real-time sensing an optoelectcial signal from the solid state device.

35. The method as in claim 34 including controlling the interfacial rectifying region to have a shallow depth of less than 70 nonometers.